Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously Presented) A method, comprising:

detecting a user initiated event in a computing system, the computing system including an integrated circuit having multiple states of performance including a first state of performance, a second state of performance higher than the first state of performance, and a third state of performance higher than the second state of performance, the computing system having a power supply which includes a battery;

directly transitioning the integrated circuit from the first state of performance to the third state of performance based upon detecting the user initiated event; and

operating the integrated circuit at the third state of performance for a period of time predetermined by thermal failure characteristics pertaining to the integrated circuit.

2. (Original) The method of claim 1, wherein the user event is defined by a programming environment within which the computing system is operating.

3. (Original) The method of claim 1, wherein directly transitioning comprises transitioning without delay.

4. (Cancelled)

5. (Previously Presented) The method of claim 1, wherein the computing system comprises a laptop computer.

6. (Original) The method of claim 1, wherein the computing system comprises a personal digital assistant.

7. (Previously Presented) An apparatus, comprising:

a computer readable medium;

a first integrated circuit having multiple states of performance including a first state of performance, a second state of performance higher than the first state of performance, and a third state of performance higher than the second state of performance, the first integrated circuit coupled to the computer readable medium; and

a program stored in the computer readable medium to manage power consumption within the first integrated circuit, instructions associated with the program to directly transition the first integrated circuit from the first state of performance to the third state of performance based upon detecting a user initiated event and to operate the integrated circuit at the third state of performance for a period of time predetermined by thermal failure characteristics pertaining to the integrated circuit.

8. (Original) The apparatus of claim 7, wherein the first state of performance comprises a first voltage level and a first operating frequency.

9. (Original) The apparatus of claim 7, wherein the third state of performance comprises a second integrated circuit co-processing instructions with the first integrated circuit.

10. (Original) The apparatus of claim 7, further comprising:

frequency regulation logic to change an operating frequency of the first integrated circuit, the frequency regulation logic to receive a signal from the program.

11. (Original) The apparatus of claim 7, further comprising:

voltage regulation logic to change an operating voltage of the first integrated circuit, the voltage regulation logic to receive a signal from the program.

12. (Original) The apparatus of claim 7, wherein the instructions reside in a Basic Input Output System.

13. (Original) The apparatus of claim 7, wherein the instructions reside in an operating system.

14. (Original) The apparatus of claim 7, wherein the instructions reside in application software.

15. (Original) The apparatus of claim 7, wherein the first integrated circuit comprises a chip set.

16. (Original) The apparatus of claim 7, wherein the first integrated circuit comprises a processing unit.

17. (Original) The apparatus of claim 12, wherein the Basic Input Output System to receive a notification signal from an operating system that the user event has occurred.

18. (Original) The apparatus of claim 11, wherein the program comprises an increasing state transition algorithm discrete from a decreasing state transition algorithm.

19. (Original) The apparatus of claim 7, wherein the program to transition the first integrated circuit to a next higher state of performance based upon an occurrence of a non-user event increasing utilization of the first integrated circuit over a preset threshold.

20. (Previously Presented) A machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform operations comprising:

detecting a user event in a computing system; the computing system including an integrated circuit having multiple states of performance including a first state of performance, a second state of performance higher than the first state of performance, and a third state of performance higher than the second state of performance;

directly transitioning the integrated circuit from the first state of performance to the third state of performance based upon detecting the user initiated event; and

operating the integrated circuit at the third state of performance for a period of time predetermined by thermal failure characteristics pertaining to the integrated circuit.

21. (Original) The machine-readable medium of claim 20, further comprising instructions which, when executed by the machine, cause the machine to perform the further operations comprising:

changing an operating frequency of the integrated circuit to change the state of performance of the integrated circuit.

22. (Original) The machine-readable medium of claim 20, further comprising instructions which, when executed by the machine, cause the machine to perform the further operations comprising:

changing an operating voltage level of the integrated circuit to change the state of performance of the integrated circuit.

23. (Previously Presented) The machine-readable medium of claim 20, further comprising instructions which, when executed by the machine, cause the machine to perform the further operations comprising:

operating the integrated circuit at the second state of performance for non-user initiated events.

24. (Previously Presented) An apparatus, comprising:

means for detecting a user event in a computing system; the computing system including an integrated circuit having multiple states of performance including a first state of performance, a second state of performance higher than the first state of performance, and a third state of performance higher than the second state of performance;

means for directly transitioning the integrated circuit from the first state of performance to the third state of performance based upon detecting the user initiated event; and

means for operating the integrated circuit at the third state of performance for a period of time predetermined by thermal failure characteristics pertaining to the integrated circuit.

25. (Original) The apparatus of claim 24, further comprising:

means for changing an operating frequency of the integrated circuit to change the state of performance of the integrated circuit.

26. (Original) The apparatus of claim 24, further comprising:

means for changing an operating voltage level of the integrated circuit to change the state of performance of the integrated circuit.

27. (Previously Presented) A machine-readable medium to provide instructions, the instructions when executed by a machine, cause the machine to perform operations comprising:

detecting a user initiated event in a computing system being powered by a battery; the computing system including an integrated circuit having multiple states of performance including a first state of performance and a highest state of performance; and

directly transitioning the integrated circuit from the first state of performance to the highest state of performance based upon detecting the user initiated event; and

operating the integrated circuit at the highest state of performance for a period of time predetermined by thermal failure characteristics pertaining to the integrated circuit.

28. (Original) The machine-readable medium of claim 27, further comprising instructions which, when executed by the machine, cause the machine to perform the further operations comprising:

changing the state of performance of the integrated circuit by changing an amount of processors to manage the processing load.

29. (Original) The machine-readable medium of claim 27, further comprising instructions which, when executed by the machine, cause the machine to perform the further operations comprising:

changing the state of performance of the integrated circuit by changing an operating frequency level of the integrated circuit.

30. (Previously Presented) An apparatus, comprising:

a first integrated circuit having multiple states of performance including a first state of performance, a second state of performance higher than the first state of performance, and a third state of performance higher than the second state of performance, the first integrated circuit; and

a power manager to manage power consumption within the first integrated circuit, the power manager to directly transition the first integrated circuit from the first state of performance to the third state of performance based upon detecting a user initiated event and to operate the integrated circuit at the third state of performance for a period of time predetermined by thermal failure characteristics pertaining to the integrated circuit.

31. (Original) The apparatus of claim 30, wherein the first state of performance comprises a first voltage level and a first operating frequency.

32. (Original) The apparatus of claim 30, wherein the third state of performance comprises a second integrated circuit co-processing instructions with the first integrated circuit.

33. (Original) The apparatus of claim 30, further comprising:

frequency regulation logic to change an operating frequency of the first integrated circuit, the frequency regulation logic to receive a signal from the program.

34. (New) The method of claim 1, wherein after the operating the integrated circuit at the third state of performance, preventing the integrated circuit from operating in the third state of performance for one or more thermal gaps, wherein each thermal gap is of a predetermined period of time based on the heat dissipation capacity of the integrated circuit.